General Description

The AAT2687 provides two independently regulated DC outputs; consisting of a high voltage step-down regulator and a low input voltage low dropout (LDO) regulator. The PMIC is optimized for low-cost 12V adapter inputs, making the device the ideal system-on-a-chip power solution for consumer communications equipment.

Channel 1 is a step-down regulator with an input voltage range 6.0 to 24V, providing up to 4.5A output current. 490kHz fixed switching frequency allows small L/C filtering components. Channel 1 utilizes voltage mode control configured for optimum performance across the entire output voltage and load range.

Channel 2 is a low-dropout (LDO) regulator providing up to 600mA output current. The device provides extremely low output noise, low quiescent current and excellent transient response.

The controller includes integrated cycle-by-cycle over-current protection, soft-start and over-temperature disable features. Independent input and enable pins provide maximum design flexibility.

The AAT2687 is available in the Pb-free, 4x5mm 24-pin TQFN package. The rated operating temperature range is -40°C to 85°C.

Features

- 2-Output Step-Down Converters:
  - Channel 1 Step-Down: \( V_{\text{IN1}} = 6V \) to 24V
  - \( V_{\text{OUT1}} \) Adjustable from 1.5V to 5.5V
  - \( I_{\text{OUT1}} \) up to 4.5A
  - High Switching Frequency
  - Voltage Mode Control
  - PWM Fixed Frequency for Low-Ripple
  - Channel 2 (LDO): \( V_{\text{IN2}} = 2.7V \) to 5.5V
  - \( I_{\text{OUT2}} \) up to 600mA
  - 1V Dropout Voltage at 600mA
  - High Accuracy \( \pm1.5\% \)

- Small Solution Size
- System On a Chip
- Ultra-small External L/C
- Shutdown Current < 35\( \mu \)A
- Independent Enable Pins
- Programmable Over-Current Protection
- Over-Temperature Protection
- Internal Soft Start
- 4x5mm 24-Pin TQFN Low Profile Thermally Enhanced Package
- -40°C to 85°C Temperature Range

Applications

- DSL and Cable Modems
- Notebook Computers
- Satellite Settop Box
- Wireless LAN Systems

Typical Application
## Pin Descriptions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LX1</td>
<td>Channel 1 step-down converter switching pin. Connect output inductor to this pin. Connect all four LX1 pins together.</td>
</tr>
<tr>
<td>2</td>
<td>LX1</td>
<td>Channel 1 step-down converter switching pin. Connect output inductor to this pin. Connect all four LX1 pins together.</td>
</tr>
<tr>
<td>3, 4</td>
<td>N/C</td>
<td>No Connect. Can be used to route IN1 and EP.</td>
</tr>
<tr>
<td>5</td>
<td>BST1</td>
<td>Channel 1 step-down regulator boost drive input pin. Connect the cathode of fast rectifier from this pin and connect a 100nF capacitor from this pin to the channel 1 switching node (LX1) for internal high-side MOSFET gate drive.</td>
</tr>
<tr>
<td>6</td>
<td>EN1</td>
<td>Channel 1 step-down regulator enable input pin. Active high enables the channel 1 output. It can be tied to VIN1.</td>
</tr>
<tr>
<td>7</td>
<td>GND2</td>
<td>Ground pin for Channel 2. Power return pin for channel 2. Connect return of channel 2 input and output capacitors close to this pin for best noise performance.</td>
</tr>
<tr>
<td>8</td>
<td>EN2</td>
<td>Channel 2 linear low dropout (LDO) enable input pin. Active high enables the channel 2 output. It can be tied to VOUT1.</td>
</tr>
<tr>
<td>9</td>
<td>N/C</td>
<td>No Connect. Can be used to route IN2.</td>
</tr>
<tr>
<td>10</td>
<td>IN2</td>
<td>Input supply voltage pin for channel 2 linear low dropout (LDO) regulator. Connect a 2.2μF ceramic input capacitor close to this pin.</td>
</tr>
<tr>
<td>11</td>
<td>OUT2</td>
<td>Output of channel 2 of linear low dropout (LDO) regulator. Connect a 2.2μF ceramic capacitor from this pin to GND pin.</td>
</tr>
<tr>
<td>12</td>
<td>N/C</td>
<td>No Connect. Can be used to route OUT2.</td>
</tr>
<tr>
<td>13</td>
<td>RS1</td>
<td>Channel 1 output current sense pin. Connect a small signal resistor from this pin to channel 1 switching node (LX) to enable over-current sense for step-down converter.</td>
</tr>
<tr>
<td>14</td>
<td>OS1</td>
<td>Channel 1 output sense voltage pin. Connect to the output capacitor to enable over-current sense for step-down converter.</td>
</tr>
<tr>
<td>15</td>
<td>COMP1</td>
<td>Compensation pin for channel 1 step-down regulator. Connect a series resistor, capacitor network to compensate the voltage mode control loop.</td>
</tr>
<tr>
<td>16</td>
<td>FB1</td>
<td>Feedback input pin for channel 1 step-down converter. Connect an external resistor divider to this pin to program the output voltage to the desired value.</td>
</tr>
<tr>
<td>17</td>
<td>GND1</td>
<td>Ground pin for Channel 1. Power return pin for channel 1. Connect return of channel 1 input and output capacitors close to this pin for best noise performance.</td>
</tr>
<tr>
<td>18</td>
<td>VL1</td>
<td>Internal linear regulator for channel 1 step-down converter. Connect a 2.2μF/6.3V capacitor from this pin to GND1 pin.</td>
</tr>
<tr>
<td>19</td>
<td>VL1</td>
<td>Internal linear regulator for channel 1 step-down converter. Connect to pin 18.</td>
</tr>
<tr>
<td>20</td>
<td>N/C</td>
<td>No Connect. Do not connect to any node on the PCB.</td>
</tr>
<tr>
<td>21</td>
<td>N/C</td>
<td>No Connect. Can be connected to GND.</td>
</tr>
<tr>
<td>22</td>
<td>IN1</td>
<td>Input supply voltage pin for channel 1 step-down regulator. Connect both IN1 pins together. Connect the input capacitor close to this pin for best noise performance.</td>
</tr>
<tr>
<td>23</td>
<td>LX1</td>
<td>Channel 1 step-down converter switching pin. Connect output inductor to this pin. Connect all four LX1 pins together.</td>
</tr>
<tr>
<td>24</td>
<td>LX1</td>
<td>Channel 1 step-down converter switching pin. Connect output inductor to this pin. Connect all four LX1 pins together.</td>
</tr>
</tbody>
</table>
Pin Configuration

TQFN45-24 (Top View)

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN1}, V_{EN1}$</td>
<td>IN1, LX, EN1 to GND</td>
<td>-0.3 to 30.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN2}$</td>
<td>IN2, VL1, OUT2 to GND</td>
<td>-0.3 to 6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BST1-LX1}$</td>
<td>BST1 to LX1</td>
<td>-0.3 to 6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CONTROL}$</td>
<td>FB1, COMP1, RS1, OS1, OUT2 to GND</td>
<td>-0.3 to $V_{IN1,LO} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EN2}$</td>
<td>EN2 to GND</td>
<td>-0.3 to $V_{IN2} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN1\text{(PULSED)}}$</td>
<td>IN1 to LX1</td>
<td>12.0</td>
<td>A</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating Junction Temperature Range</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{LEAD}$</td>
<td>Maximum Soldering Temperature (at leads, 10 sec)</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>

Thermal Information

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Theta_{JA}$</td>
<td>Thermal Resistance$^2$</td>
<td>33</td>
<td>°C/W</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Maximum Power Dissipation$^3$</td>
<td>3.0</td>
<td>W</td>
</tr>
</tbody>
</table>

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board with exposed paddle connected to ground plane.
3. Derate 30 mW/°C above 25°C ambient temperature.
**Electrical Characteristics**\(^1\)

\(V_{\text{IN1}} = 12.0\, \text{V}, \, V_{\text{IN2}} = 3.3\, \text{V}; \, T_a = -40^\circ\text{C} \text{ to } 85^\circ\text{C}, \) unless noted otherwise. Typical values are at \(T_a = 25^\circ\text{C}.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Channel 1: Step-Down Converter</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{IN}})</td>
<td>Input Voltage</td>
<td>(V_{\text{IN}}, , \text{Rising})</td>
<td>6.0</td>
<td>24.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{UVLO}})</td>
<td>UVLO Threshold</td>
<td>(V_{\text{IN}}, , \text{Hysteresis})</td>
<td>3.0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OUT1}})</td>
<td>Output Voltage Range</td>
<td></td>
<td>1.5</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{REF1}})</td>
<td>Feedback Pin Voltage</td>
<td>(T_a = 25^\circ\text{C})</td>
<td>0.591</td>
<td>0.600</td>
<td>0.609</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OUT}})</td>
<td>Output Voltage Accuracy</td>
<td>(I_{\text{OUT1}} = 0, \text{A to } 4.5, \text{A})</td>
<td>-2.5</td>
<td>2.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{\text{OUT}}/V_{\text{OUT}})</td>
<td>Line Regulation</td>
<td>(V_{\text{IN1}} = 6, \text{V to } 24, \text{V}, , V_{\text{OUT1}} = 3.3, \text{V}, , I_{\text{OUT1}} = 4.5, \text{A})</td>
<td>0.06</td>
<td>%/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{\text{OUT}}/V_{\text{IN}})</td>
<td>Load Regulation</td>
<td>(V_{\text{OUT1}} = 12, \text{V}, , V_{\text{IN1}} = 3.3, \text{V}, , I_{\text{OUT1}} = 0, \text{A to } 4.5, \text{A})</td>
<td>0.18</td>
<td>%/A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{\text{Q1}})</td>
<td>Quiescent Current</td>
<td>(V_{\text{EN1}} = \text{High, No load})</td>
<td>0.6</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{SHD}})</td>
<td>Shutdown Current</td>
<td>(V_{\text{EN1}} = \text{Low, } V_{\text{L1}} = 0, \text{V})</td>
<td>35.0</td>
<td>(\mu)A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OCP1}})</td>
<td>Over-Current Offset Voltage</td>
<td>(V_{\text{EN1}} = \text{High, } V_{\text{IN1}} = 6.0, \text{V to } 24.0, \text{V}, , T_a = 25^\circ\text{C})</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>mV</td>
</tr>
<tr>
<td>(V_{\text{LM1}})</td>
<td>LX Pin Leakage Current</td>
<td>(V_{\text{EN1}} = 24.0, \text{V}, , V_{\text{EN1}} = \text{Low})</td>
<td>-1.0</td>
<td>1.0</td>
<td>(\mu)A</td>
<td></td>
</tr>
<tr>
<td>(T_{\text{DMAX}})</td>
<td>Maximum Duty Cycle</td>
<td></td>
<td>85</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{\text{ON}})</td>
<td>Minimum On-Time</td>
<td>(V_{\text{IN1}} = 6.0 \text{ to } 24.0, \text{V})</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_{\text{DSON}})</td>
<td>High Side On-Resistance</td>
<td>(V_{\text{L1}} = 4.5, \text{V})</td>
<td>35</td>
<td>(\mu)Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(F_{\text{OSC1}})</td>
<td>Oscillator Frequency</td>
<td></td>
<td>350</td>
<td>490</td>
<td>650</td>
<td>kHz</td>
</tr>
<tr>
<td>(F_{\text{FOLDBACK1}})</td>
<td>Short Circuit Foldback Frequency</td>
<td>Current Limit Triggered</td>
<td>100</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{\text{S2}})</td>
<td>Start-Up Time</td>
<td>From Enable Channel 1 to Output Regulation</td>
<td>2.5</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel 2: 600mA Linear Low Dropout (LDO) Regulator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{IN2}})</td>
<td>Input Voltage</td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{D02}})</td>
<td>Dropout Voltage</td>
<td>(98% \times V_{\text{OUT2, NORM}}, , I_{\text{OUT2}} = 600, \text{mA})</td>
<td>1000</td>
<td>1300</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{Q2}})</td>
<td>Quiescent (Ground) Current</td>
<td>No load</td>
<td>70</td>
<td>125</td>
<td>(\mu)A</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{SHDN2}})</td>
<td>Shutdown Current</td>
<td>(V_{\text{EN2}} = \text{GND})</td>
<td>1.0</td>
<td>(\mu)A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OUT2(TOL1)}})</td>
<td>Output Voltage Tolerance</td>
<td>(I_{\text{OUT2}} = 1, \text{mA to } 600, \text{mA}, , V_{\text{IN2}} = 2.7, \text{V to } 5.5, \text{V}, , T_a = 25^\circ\text{C})</td>
<td>-2.0</td>
<td>+2.0</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OUT2(TOL1)}})</td>
<td>Output Voltage Tolerance</td>
<td>(I_{\text{OUT2}} = 1, \text{mA to } 600, \text{mA}, , V_{\text{IN2}} = 2.7, \text{V to } 5.5, \text{V}, , T_a = -40^\circ\text{C to } 85^\circ\text{C})</td>
<td>-3.5</td>
<td>+3.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>(e_{n})</td>
<td>Output Noise</td>
<td>(\text{BW = 300Hz to } 50, \text{kHz})</td>
<td>250</td>
<td>(\mu)V_\text{RMS}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio</td>
<td>(I_{\text{OUT2}} = 10, \text{mA})</td>
<td>67</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{LMT2}})</td>
<td>Current Limit</td>
<td></td>
<td>700</td>
<td>800</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(T_{\text{S2}})</td>
<td>Enable Start-Up Delay</td>
<td>From Enable Channel 2 to Output Regulation</td>
<td>15</td>
<td>(\mu)s</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Over-Temperature, EN Logic</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{\text{SD1,2}})</td>
<td>Over-Temperature Shutdown Threshold</td>
<td></td>
<td>135</td>
<td>(^\circ)C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{\text{SD1,2}})</td>
<td>Over-Temperature Shutdown Hysteresis</td>
<td></td>
<td>15</td>
<td>(^\circ)C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{EN1,EN2(L)}})</td>
<td>Enable Threshold Low</td>
<td></td>
<td>0.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{EN1,EN2(H)}})</td>
<td>Enable Threshold High</td>
<td></td>
<td>2.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{EN2(H)}})</td>
<td>Enable Threshold High</td>
<td></td>
<td>1.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{\text{EN1,EN2}})</td>
<td>Input Low Current</td>
<td></td>
<td>-1.0</td>
<td>1.0</td>
<td>(\mu)A</td>
<td></td>
</tr>
</tbody>
</table>

1. The AAT2687 is guaranteed to meet performance specifications over the \(-40^\circ\text{C to } +85^\circ\text{C}\) operating temperature range and is assured by design, characterization and correlation with statistical process controls.
Typical Characteristics—Channel 1

### Step-Down Converter Efficiency vs. Load Current

![Graph showing efficiency vs. load current for different input voltages.](image)

- **V_{IN1} = 6V**
- **V_{IN1} = 7V**
- **V_{IN1} = 8V**
- **V_{IN1} = 12V**
- **V_{IN1} = 18V**
- **V_{IN1} = 24V**

### Step-Down Converter Load Regulation vs. Load Current

![Graph showing load regulation vs. load current for different input voltages.](image)

- **V_{IN1} = 6V**
- **V_{IN1} = 7V**
- **V_{IN1} = 8V**
- **V_{IN1} = 12V**
- **V_{IN1} = 18V**
- **V_{IN1} = 24V**

### Step-Down Converter Line Regulation vs. Load Current

![Graph showing line regulation vs. load current for different input voltages.](image)

- **I_{OUT1} = 0.1\mu A**
- **I_{OUT1} = 2.25A**
- **I_{OUT1} = 3.5A**
- **I_{OUT1} = 4mA**
- **I_{OUT1} = 4.5A**

### No Load Step-Down Converter Input Current vs. Input Voltage

![Graph showing no load input current vs. input voltage.](image)

- **85°C**
- **25°C**
- **-40°C**

### Step-Down Converter Switching Frequency vs. Input Voltage

![Graph showing switching frequency vs. input voltage.](image)

- **85°C**
- **25°C**
- **-40°C**

### Step-Down Converter Output Voltage vs. Temperature

![Graph showing output voltage vs. temperature.](image)

- **V_{OUT} = 3.3V; I_{OUT1} = 4.5A; C_{OUT1} = 66\mu F; L = 4.7\mu H; V_{IN1} = 12V**

DISCONTINUED
Typical Characteristics—Channel 1

Step-Down Converter Load Transient
(V_{OUT1} = 3.3V; V_{IN1} = 12V; C_{OUT1} = 66\mu F; L = 4.7\mu H)

Step-Down Converter Output Voltage Ripple
(V_{OUT1} = 3.3V; V_{IN1} = 12V; C_{OUT1} = 66\mu F; L = 4.7\mu H; I_{OUT1} = 4.5A)

Step-Down Converter Load Transient
(V_{OUT1} = 3.3V; V_{IN1} = 12V; C_{OUT1} = 66\mu F; L = 4.7\mu H)

Step-Down Converter Line Transient
(V_{OUT1} = 3.3V; C_{OUT1} = 66\mu F; L = 4.7\mu H)

Step-Down Converter Output Voltage Ripple
(V_{OUT1} = 3.3V; V_{IN1} = 12V; C_{OUT1} = 66\mu F; L = 4.7\mu H; I_{OUT1} = 1mA)

Time (100\mu s/div)

Time (100\mu s/div)

Time (1\mu s/div)

Time (2\mu s/div)

DISCONTINUED
Typical Characteristics—Channel 2

**LDO Input Current vs. Input Voltage**

(\(V_{\text{EN1}} = 0\V; \ V_{\text{EN2}} = \ V_{\text{IN2}}\))

**LDO Dropout Voltage vs. Temperature**

\(I_{\text{OUT2}} = \) 600mA, 500mA, 50mA

**LDO Dropout Voltage vs. Output Current**

\(I_{\text{OUT2}} = \) 600mA, 50mA

**LDO VIH and VIL vs. Input Voltage**

\(V_{\text{IN2}} = 3.3\V; \ V_{\text{OUT2}} = 1.8\V; \ I_{\text{OUT2}} = 600\mA\)

**LDO Output Voltage Error vs. Temperature**

\(V_{\text{OUT2}} = 1.8\V\)

**LDO Dropout Characteristic**

\(V_{\text{OUT2}} = 1.8\V\)
Typical Characteristics—Channel 2

LDO Turn-Off Response Time
(VIN2 = 3.3V; VEN2 = 3.3V; VOUT2 = 1.8V; IOUT2 = 600mA)

Time (5µs/div)

Enable Voltage (top) (V)
Output Voltage (bottom) (V)

LDO Turn-On Time from Enable
(VIN2 = 3.3V; VEN2 = 3.3V; VOUT2 = 1.8V; IOUT2 = 600mA)

Time (5µs/div)

Enable Voltage (top) (V)
Output Voltage (bottom) (V)

LDO Line Transient Response
(VIN2 = 3V to 4V; VOUT2 = 1.8V; IOUT2 = 600mA; COUT2 = 2.2µF)

Time (200µs/div)

Input Voltage (top) (V)
Output Voltage (bottom) (V)

LDO Load Transient Response
(IOUT2 = 0.3 to 0.6A; VIN2 = 3.3V; VOUT2 = 1.8V; COUT2 = 2.2µF)

Time (40µs/div)

Output Current (top) (A)
Output Voltage (bottom) (V)

LDO Output Voltage Noise
(IOUT2 = 10mA; Power BW: 300~50KHz)

Magnitude (μVRMS)
Frequency (Hz)

LDO Power Supply Rejection Ratio, PSRR
(IOUT2 = 10mA; BW: 100KHz to 300KHz)

Magnitude (dB)
Frequency (Hz)
**Functional Description**

The AAT2687 provides two independently regulated DC outputs, consisting of a high voltage step-down regulator and a low input voltage linear low dropout (LDO) regulator. The PMIC is optimized for low cost 12V adapter inputs, making the device an ideal system-on-a-chip power solution for consumer communications equipment.

Channel 1 is a step-down regulator with an input voltage range 6.0 to 24V, providing up to 4.5A output current. The 490kHz fixed switching frequency allows small L/C filtering components.

Channel 1 utilizes voltage mode control configured for optimum performance across the entire output voltage and load range. The controller includes integrated over-current, soft-start and over-temperature protection. Over-current is sensed through the output inductor DC winding resistance (DCR). An external resistor network adjusts the current limit according to the DCR of the desired inductor and the desired output current limit. Frequency reduction limits over-current stresses during short-circuit events. The operating frequency returns to the nominal setting when over-current conditions are removed.

Channel 2 is a linear low-dropout (LDO) regulator providing up to 600mA output current at a factory set output voltage. The device provides extremely low output noise, low quiescent current and excellent transient response.

The controller includes integrated over-current, soft-start and over-temperature protection. Independent input and enable pins provide maximum design flexibility. The AAT2687 is available in the Pb-free, 4x5mm 24-pin TQFN package. The rated operating temperature range is -40°C to 85°C.
Applications Information

Output 1 is a high voltage DC/DC step-down converter providing an output voltage from 1.5V to 85% of the minimum input voltage (85% \cdot V_{IN}). The integrated high-side n-channel MOSFET device provides up to 4.5A output current. Input voltage range is 6.0V to 24.0V. The step-down converter utilizes constant frequency (PWM-mode) voltage mode control to achieve high operating efficiency while maintaining extremely low output noise across the operating range. High 490kHz (nominal) switching frequency allows small external filtering components; achieving minimum cost and solution size. External compensation allows the designer to optimize the transient response while achieving stability across the operating range.

Output 2 is a low voltage, low dropout (LDO) linear regulator providing 1.8V with up to 600mA output current. The input voltage range is 2.7V to 5.5V. The LDO provides very low noise output which can be derived directly from the Output 1 channel.

Channel 1 Output Voltage and Current

Output 1 is set using an external resistor divider as shown in Table 1. Minimum output voltage is 1.5V and maximum output voltage is 5.5V. Typical maximum duty cycle is 85%.

<table>
<thead>
<tr>
<th>( V_{OUT} ) (V)</th>
<th>( R_3 ) (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>2.94</td>
</tr>
<tr>
<td>1.8</td>
<td>3.92</td>
</tr>
<tr>
<td>1.85</td>
<td>4.02</td>
</tr>
<tr>
<td>2.0</td>
<td>4.53</td>
</tr>
<tr>
<td>2.5</td>
<td>6.19</td>
</tr>
<tr>
<td>3.0</td>
<td>7.87</td>
</tr>
<tr>
<td>3.3</td>
<td>8.87</td>
</tr>
<tr>
<td>5.0</td>
<td>14.3</td>
</tr>
</tbody>
</table>

Table 1: Feedback Resistor Values.

Alternatively, the feedback resistor may be calculated using the following equation:

\[
R_3 = \frac{(V_{OUT} - 0.6) \cdot R_4}{0.6}
\]

\( R_3 \) is rounded to the nearest 1% resistor value.

Channel 1 Regulator Output Capacitor Selection

Three 22μF ceramic output capacitors are required to filter the inductor current ripple and supply the load transient current for \( I_{OUT} = 4.5A \). The 1206 package with 10V minimum voltage rating is recommended for the output capacitors to maintain a minimum capacitance drop with DC bias.

Channel 1 Output Inductor Selection

The step-down converter utilizes constant frequency (PWM-mode) voltage mode control. A 4.7μH inductor value is selected to maintain the desired output current ripple and minimize the converter’s response time to load transients. The peak switch current should not exceed the inductor saturation current, the MOSFET or the external Schottky rectifier peak current ratings.

Channel 1 Rectifier Selection

When the high-side switch is on, the input voltage will be applied to the cathode of the Shottky diode. The rectifier's rated reverse breakdown voltage must be chosen at least equal to the maximum input voltage of the step-down regulator.

When the high-side switch is off, the current will flow from the power ground to the output through the Schottky diode and the inductor. The power dissipation of the Schottky diode during the time-off can be determined by the following equation:

\[
P_D = I_{OUT} \cdot V_D \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)
\]

Where \( V_D \) is the voltage drop across the Schottky diode.

Channel 1 Input Capacitor Selection

For low cost applications, a 220μF/25V electrolytic capacitor is selected to control the voltage overshoot across the high side MOSFET. A small ceramic capacitor with voltage rating at least 1.05 times greater than the maximum input voltage is connected as close as possible to the input pin (Pin 14) for high frequency decoupling.
The transfer function of the Error Amplifier is dominated by the DC Gain and the $L \cdot C_{OUT}$ output filter of the regulator. This output filter and its equivalent series resistor (ESR) create a double pole at $F_{LC}$ and a zero at $F_{ESR}$ in the following equations:

**Eq. 1:**
$$F_{LC} = \frac{1}{2 \cdot \pi \cdot L \cdot C_{OUT}}$$

**Eq. 2:**
$$F_{ESR} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}}$$

The feedback and compensation networks provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin for system stability. Equations 3, 4, 5 and 6 relate the compensation network’s poles and zeros to the components $R_1$, $R_3$, $R_5$, $C_5$, $C_6$, and $C_{10}$:

**Eq. 3:**
$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_5}$$

**Eq. 4:**
$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot (R_3 + R_5) \cdot C_{10}}$$

**Eq. 5:**
$$F_{P1} = \frac{1}{2 \cdot \pi \cdot R_1 \cdot \left(\frac{C_5 \cdot C_{6}}{C_5 + C_{6}}\right)}$$

**Eq. 6:**
$$F_{P2} = \frac{1}{2 \cdot \pi \cdot R_5 \cdot C_{10}}$$

Components of the feedback, feed forward, compensation, and current limit networks need to be adjusted to maintain the system’s stability for different input and output voltages applications as shown in Table 1.

**Channel 1 Thermal Protection**

The AAT2687 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 135°C. The internal thermal protection circuit will actively turn off the high side regulator output device to prevent the possibility of over temperature damage. The Buck regulator output will remain in a shutdown state until the internal die temperature falls back below the 135°C trip point. The combination and interaction between the short circuit and thermal protection systems allows the Buck regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

<table>
<thead>
<tr>
<th>Network</th>
<th>Components</th>
<th>$V_{OUT}=3.3V$ $V_{IN}=6V-24V$</th>
<th>$V_{OUT}=5.0V$ $V_{IN}=6V-24V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback</td>
<td>$R_4$</td>
<td>1.96kΩ</td>
<td>1.96kΩ</td>
</tr>
<tr>
<td></td>
<td>$R_3$</td>
<td>8.87kΩ</td>
<td>8.87kΩ</td>
</tr>
<tr>
<td></td>
<td>$C_{10}$</td>
<td>2.2nF</td>
<td>2.2nF</td>
</tr>
<tr>
<td>Feed-forward</td>
<td>$R_5$</td>
<td>453Ω</td>
<td>453Ω</td>
</tr>
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<td>2.2nF</td>
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<td>$C_6$</td>
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<td>150pF</td>
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<td></td>
<td>$R_1$</td>
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<td>3.92kΩ</td>
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<tr>
<td>Compensation</td>
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<td>220nF</td>
<td>220nF</td>
</tr>
<tr>
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</tr>
<tr>
<td></td>
<td>$R_8$</td>
<td>165kΩ</td>
<td>165kΩ</td>
</tr>
</tbody>
</table>

Table 1: AAT2687 Feedback, Compensation, and Current Limit Components For $V_{OUT}=3.3V$ and $V_{OUT}=5.0V$.  

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Over-Current Protection

The output 1 controller provides true-load DC output current sensing which protects the load and limits component stresses. The output current is sensed through the DC resistance in the output inductor (DCR). The controller reduces the operating frequency when an over-current condition is detected; limiting stresses and preventing inductor saturation. This allows the smallest possible inductor for a given output load. A small resistor divider may be necessary to adjust the over-current threshold and compensate for variation in inductor DCR.

The preset current limit threshold is triggered when the differential voltage from RS1 to OS1 exceeds 100mV (nominal).

Channel 2 Input Capacitor

Typically, a 1μF or larger capacitor is recommended for C_in in most applications. A C_in capacitor is not required for basic LDO regulator operation. However, if the AAT2687 is physically located more than three centimeters from an input power source, a C_in capacitor will be needed for stable operation.

C_in should be located as close to the device V_IN pin as possible. C_in values greater than 1μF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_in. There is no specific capacitor ESR requirement for C_in. However, for 150mA LDO regulator output operation, ceramic capacitors are recommended for C_in due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources, such as batteries in portable devices.

Channel 2 Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins V_OUT and GND. The C_out capacitor connection to the LDO regulator ground pin should be connected as close as possible for maximum device performance. The AAT2687 LDO has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1μF to 10μF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the channel 2 should use 2.2μF or greater for C_out. If desired, C_out may be increased without limit. In low output current applications where output load is less than 10mA, the minimum value for C_out can be as low as 0.47μF.

Channel 2 Enable Function

The AAT2687 features an LDO regulator enable/disable function. This pin (EN) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_IN to keep the LDO regulator in a continuously on state. When the LDO regulator is in shut-
down mode, an internal 1.5kΩ resistor is connected between V\textsubscript{OUT} and GND. This is intended to discharge C\textsubscript{OUT} when the LDO regulator is disabled. The internal 1.5kΩ has no adverse effect on device turn-on time.

**Channel 2 Short-Circuit Protection**

The AAT2687 LDO contains an internal short-circuit protection circuit that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or LDO regulator package power dissipation exceeds the device thermal limit.

**Channel 2 Thermal Protection**

The AAT2687 LDO has an internal thermal protection circuit which will turn on when the device die temperature exceeds 150°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of over temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 150°C trip point. The combination and interaction between the short circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

**Channel 2 No-Load Stability**

The AAT2687 is designed to maintain output voltage regulation and stability under operational no load conditions. This is an important characteristic for applications where the output current may drop to zero.

**Channel 2 Reverse Output-to-Input Voltage Conditions and Protection**

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage, maintaining a reverse bias on the internal parasitic diode. Conditions where V\textsubscript{OUT} might exceed V\textsubscript{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V\textsubscript{OUT} pin, possibly damaging the LDO regulator. In applications where there is a possibility of V\textsubscript{OUT} exceeding V\textsubscript{IN} for brief amounts of time during normal operation, the use of a larger value C\textsubscript{IN} capacitor is highly recommended. A larger value of C\textsubscript{IN} with respect to C\textsubscript{OUT} will effect a slower C\textsubscript{IN} decay rate during shutdown, thus preventing V\textsubscript{OUT} from exceeding V\textsubscript{IN}. In applications where there is a greater danger of V\textsubscript{OUT} exceeding V\textsubscript{IN} for extended periods of time, it is recommended to place a Schottky diode across V\textsubscript{IN} to V\textsubscript{OUT} (connecting the cathode to V\textsubscript{IN} and anode to V\textsubscript{OUT}). The Schottky diode forward voltage should be less than 0.45V.

**Thermal Calculations**

There are three types of losses associated with the AAT2687 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the R\textsubscript{DS(ONX)} characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the synchronous step-down converter and LDO losses is given by:

\[
P_{\text{TOTAL}} = I_{\text{OUT1}}^2 \cdot \left( R_{\text{DS(ONH)}} \cdot V_{\text{OUT1}} + R_{\text{DS(ONL)}} \cdot (V_{\text{IN1}} - V_{\text{OUT1}}) \right) + (t_{\text{SW}} \cdot F_S \cdot I_{\text{OUT1}} + I_{\text{Q1}}) \cdot V_{\text{IN1}} + (V_{\text{IN2}} - V_{\text{OUT2}}) \cdot I_{\text{OUT2}}
\]

I\textsubscript{Q1} and I\textsubscript{Q2} are the step-down converter and LDO quiescent currents respectively. The term t\textsubscript{SW} is used to estimate the full load step-down converter switching losses.

For asynchronous Step-Down converter, the power dissipation is only in the internal high side MOSFET during the on time. When the switch is off, the power dissipates on the external Schottky diode. The total package losses for the AAT2687 reduce to the following equation:

\[
P_{\text{TOTAL}} = I_{\text{OUT1}}^2 \cdot R_{\text{DS(ONH)}} \cdot D + (t_{\text{SW}} \cdot F_S \cdot I_{\text{OUT1}} + I_{\text{Q2}}) \cdot V_{\text{IN}} + (V_{\text{IN2}} - V_{\text{OUT2}}) \cdot I_{\text{OUT2}}
\]

Where: D = \frac{V_{\text{OUT}}}{V_{\text{IN}}} is the duty cycle.

Since R\textsubscript{DS(ONX)} quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the \( \theta_{JA} \) for the TQFN45-24 package, which is 33°C/W.

\[
T_{J(\text{MAX})} = P_{\text{TOTAL}} \cdot \theta_{JA} + T_{\text{AMB}}
\]
Layout Considerations

The suggested PCB layout for the AAT2687 is shown in Figures 5, 6, 7, and 8. The following guidelines should be used to help ensure a proper layout.

1. The power input capacitors (C1 and C15) should be connected as close as possible to high voltage input pin (IN1) and power ground.
2. C1, L1, D2, C7, C8, and C9 should be placed as close as possible to minimize any parasitic inductance in the switched current path which generates a large voltage spike during the switching interval. The connection of inductor to switching node should be as short as possible.
3. The feedback trace or FB1 pin should be separated from any power trace and connected as close as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load returns to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect unused signal pins to ground or input to avoid unwanted noise coupling.
6. The critical small signal components include feedback components, and compensation components should be placed close to the FB1 and COMP1 pins. The feedback resistors should be located as close as possible to the FB1 pin with its ground tied straight to the signal ground plane which is separated from power ground plane.
7. C4 should be connected close to the RS1 and OS1 pins, while R2 should be connected directly to the output pin of the inductor. For the best current limit performance, C4 and R2 should be placed at the bottom layer to avoid noise coupling from the inductor.
8. R7 should be connected directly to the output pin of inductor L1 to sense precisely its DCR.
9. For good thermal coupling, a 4-layer PCB layout is recommended and PCB vias are required from the exposed pad (EP) for the TQFN45-24 paddle to the middle planes and bottom plane. The EP is internally connected to IN.
**PMIC Solution for 24V Systems with 2 High Performance Step-Down Converters**

**Figure 4: AAT2687IFK Evaluation Board Schematic For VIN = 6V - 24V and VOUT = 3.3V.**
AAT2687

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with 2 High Performance Step-Down Converters

Figure 5: AAT2687IFK Evaluation Board Top Layer.

Figure 6: AAT2687IFK Evaluation Board MID1 Layer.

Figure 7: AAT2687IFK Evaluation Board MID2 Layer.

Figure 8: AAT2687IFK Evaluation Board Bottom Layer.

DISCONTINUED
AAT2687 Design Example

Specifications

- \( V_{O1} = 3.3V \) @ 4.5A, Pulsed Load \( \Delta I_{LOAD} = 4.5A \)
- \( V_{O2} = 1.8V \) @ 600mA
- \( V_{IN1} = 12V \)
- \( F_S = 490kHz \)
- \( T_{AMB} = 85°C \) in TQFN45-24 Package

Channel 1 Output Inductor

For Sumida inductor RCH108NP-4R7M, 4.7\( \mu \)H, DCR = 11.7m\( \Omega \) max.

\[
\Delta I = \frac{V_{OUT1}}{L_1 \cdot F_S} \left( 1 - \frac{V_{OUT1}}{V_{IN1}} \right) = \frac{3.3V}{4.7\mu H \cdot 490kHz} \cdot \left( 1 - \frac{3.3V}{12V} \right) = 1A
\]

\[
I_{PK1} = I_{OUT1} + \frac{\Delta I}{2} = 4.5A + 1A = 5.5A
\]

\[
P_L1 = I_{OUT1}^2 \cdot DCR = 5.5A^2 \cdot 11.7m\Omega = 354mW
\]

Channel 1 Output Capacitor

\[
V_{DROOP} = 0.4V
\]

\[
C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 4.5A}{0.4V \cdot 490kHz} = 69\mu F; \text{ use } 3 \times 22\mu F
\]

\[
I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT1} \cdot (V_{IN(MAX)} - V_{OUT1})}{L_1 \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.3V \cdot (24V - 3.3V)}{4.7\mu H \cdot 490kHz \cdot 24V} = 357mA_{RMS}
\]

\[
P_{RMS} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot (357mA)^2 = 0.6W
\]

Channel 1 Input Capacitor

Input Ripple \( V_{PP} = 33mV \)

\[
C_{IN1} = \frac{1}{\left( \frac{V_{PP}}{I_{OUT1}} - ESR \right) \cdot 4 \cdot F_S} = \frac{1}{\left( \frac{5.5mV}{4.5A} - 5m\Omega \right) \cdot 4 \cdot 490kHz} = 219\mu F
\]

For low cost applications, a 220\( \mu \)F/25V electrolytic capacitor in parallel with a 1\( \mu \)F/25V ceramic capacitor is used to reduce ESR.

\[
I_{RMS} = \frac{I_{OUT1}}{2} = 2.25A
\]

\[
P = ESR \cdot (I_{RMS})^2 = 5m\Omega \cdot (2.25A)^2 = 25.3mW
\]
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Channel 1 Current Limit
Voltage sense $V_s = 100\text{mV}$
Total trace parasitic resister and inductor DCR is $10\text{mΩ}$
$I_{\text{LIMIT}} = 5\text{A}$.

$I_{\text{PRESET}} = \frac{V_s}{\text{DCR}} = \frac{100\text{mV}}{10\text{mΩ}} = 10\text{A} > I_{\text{LIMIT}}$

$R_8 = \frac{V_{\text{OUT}} \cdot R_2}{V_s \cdot I_{\text{LIMIT}} \cdot \text{DCR}} = \frac{3.3\text{V} \cdot 2\text{kΩ}}{0.1\text{V} \cdot 6\text{A} \cdot 10\text{mΩ}} = 165\text{kΩ}$

$R_7 = \frac{R_2 \cdot R_8}{R_8 - R_2} = \frac{2\text{kΩ} \cdot 165\text{kΩ}}{165\text{kΩ} - 2\text{kΩ}} = 2\text{kΩ}$

AAT2687 Losses
All values assume 25°C ambient temperature and thermal resistor of 50°C/W in the TQFN45-24 package.

$P_{\text{TOTAL}} = I_{\text{OUT1}}^2 \cdot R_{\text{DS(on)H}} \cdot D + (t_{\text{SW}} \cdot F_s \cdot I_{\text{OUT1}} + I_0) \cdot V_{\text{IN1}} + (V_{\text{IN2}} - V_{\text{OUT2}}) \cdot I_{\text{OUT2}}$

$P_{\text{TOTAL}} = \frac{4.5\text{A}^2 \cdot 70\text{mΩ} \cdot 3.3\text{V}}{12\text{V}} + (5\text{ns} \cdot 490\text{kHz} \cdot 4.5\text{A} + 70\mu\text{A}) \cdot 12\text{V} + (3.3 \cdot 1.8) \cdot 600\text{mA}$

$P_{\text{TOTAL}} = 1.42\text{W}$

$T_{\text{J(MAX)}} = T_{\text{AMB}} + \Theta_{\text{JA}} \cdot P_{\text{LOSS}} = 85°C + (33°C/\text{W}) \cdot 1.42\text{W} = 131°C$

DISCONTINUED
Ordering Information

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<thead>
<tr>
<th>Package</th>
<th>Voltage</th>
<th>Marking¹</th>
<th>Part Number (Tape and Reel)²</th>
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Skyworks Green™ products are compliant with all applicable legislation and are halogen-free.
For additional information, refer to Skyworks Definition of Green™, document number SQ04-0074.

Legend

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<tr>
<th>Voltage</th>
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<tr>
<td>1.8</td>
<td>I</td>
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</tbody>
</table>

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in BOLD.

DISCONTINUED
PMIC Solution for 24V Systems
with 2 High Performance Step-Down Converters

Package Information

1. The leadless package family, which includes QFN, TQFN, DFN, TDFN, and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.