General Description

The AAT2688 provides two independently regulated DC outputs: a high voltage synchronous step-down (Buck) regulator and a low input voltage step-down low dropout (LDO) regulator. The PMIC is optimized for low cost 12V adapter inputs, making the device the ideal system-on-a-chip power solution for consumer communications equipment.

Channel 1 is a step-down regulator with an input voltage range of 6.0V to 24V, providing up to 4.5A output current. 490kHz fixed switching frequency allows small L/C filtering components. Channel 1 utilizes voltage mode control configured for optimum performance across the entire output voltage and load range.

Channel 2 is a low-dropout (LDO) regulator providing up to 600mA output current. The device provides low output noise, low quiescent current, and excellent transient response.

The step-down regulator includes integrated over-current, soft-start and over-temperature protection. Independent input and enable pins provide maximum design flexibility.

The AAT2688 is available in the Pb-free 4mm x 5mm 24-pin TQFN package. The rated operating temperature range is -40°C to 85°C.

Features

- 2-Output Step-Down Converters:
  - Channel 1 (Buck): \( V_{\text{IN1}} = 6.0 \text{ to } 24.0V \)
    - \( V_{\text{OUT1}} \) Adjustable from 0.8V to 5.5V
    - \( I_{\text{OUT1}} \) up to 4.5A
  - High Switching Frequency
  - Voltage Mode Control
  - High Accuracy \( \pm 1.5\% \)
  - PWM Fixed Frequency for Low Ripple
  - Channel 2 (LDO): \( V_{\text{IN2}} = 2.7V \text{ to } 5.5V \)
    - \( I_{\text{OUT2}} \) up to 600mA
    - 1V Dropout Voltage at 600mA \( I_{\text{OUT}} \)
  - Small Solution Size
  - System on a Chip
  - Ultra-small External L/C
  - Shutdown Current <35\uA
  - Independent Enable Pins
  - Over-Current and Over-Temperature Protection
  - Internal Soft Start
  - 4x5mm 24-Pin TQFN Low Profile Package
  - -40°C to 85°C Temperature Range

Applications

- DSL and Cable Modems
- Notebook Computers
- Satellite Set-top Boxes
- Wireless LAN Systems

Typical Application
## Pin Descriptions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2, 23, 24</td>
<td>LX1</td>
<td>Channel 1 step-down (Buck) converter switching pin. Connect output inductor to this pin. Connect both LX1 pins together.</td>
</tr>
<tr>
<td>3, 4, 9, 12</td>
<td>N/C</td>
<td>No connect. For optional routing reasons, pins 3 and 4 can be connected to V_in pin 9 to pin 10 (IN2), and pin 12 to pin 11 (OUT2).</td>
</tr>
<tr>
<td>5</td>
<td>BST1</td>
<td>Channel 1 step-down regulator boost drive input pin. Connect the cathode of fast rectifier from this pin and connect a 100nF capacitor from this pin to the channel 1 switching node (LX1) for internal hi-side MOSFET gate drive.</td>
</tr>
<tr>
<td>6</td>
<td>EN1</td>
<td>Channel 1 step-down regulator enable input pin. Active high enables internal linear regulator and channel 1 output.</td>
</tr>
<tr>
<td>7</td>
<td>GND2</td>
<td>Ground pin for Channel 2. Power return pin for channel 2. Connect return of channel 2 input and output capacitors close to this pin for best noise performance.</td>
</tr>
<tr>
<td>8</td>
<td>EN2</td>
<td>Channel 2 low dropout (LDO) enable input pin. Active high.</td>
</tr>
<tr>
<td>10</td>
<td>IN2</td>
<td>Input supply voltage pin for channel 2 linear low dropout (LDO) regulator. Connect 2.2 μF ceramic input capacitor close to this pin.</td>
</tr>
<tr>
<td>11</td>
<td>OUT2</td>
<td>Output of channel 2 of linear low dropout (LDO) regulator. Connect a 2.2 μF ceramic capacitor from this pin to GND pin.</td>
</tr>
<tr>
<td>13</td>
<td>RS1</td>
<td>Channel 1 output current sense pin. Connect a small signal resistor from this pin to switching node (LX1) to enable over-current sense for step-down converter. The current limit threshold varies with sense resistor sizing.</td>
</tr>
<tr>
<td>14</td>
<td>OS1</td>
<td>Channel 1 output sense voltage pin. Connect to the output capacitor to enable over-current sense for step-down converter.</td>
</tr>
<tr>
<td>15</td>
<td>COMP1</td>
<td>Compensation pin for channel 1 step-down regulator. Connect a series resistor, capacitor network to compensate the voltage mode control loop.</td>
</tr>
<tr>
<td>16</td>
<td>FB1</td>
<td>Feedback input pin for channel 1 step-down converter. Connect an external resistor divider to this pin to program the output voltage to the desired value.</td>
</tr>
<tr>
<td>17</td>
<td>GND1</td>
<td>Ground pin for channel 1. Power return pin for channel 1. Connect return of channel 1 input and output capacitors close to this pin for best noise performance.</td>
</tr>
<tr>
<td>18, 19</td>
<td>VL1</td>
<td>Internal linear regulator. Connect a 2.2 μF capacitor from this pin to GND pin.</td>
</tr>
<tr>
<td>20</td>
<td>DL1</td>
<td>Channel 1 gate drive for low side MOSFET. Connect to the gate pin of an external N type MOSFET (see the &quot;MOSFET Selection&quot; section of this product datasheet).</td>
</tr>
<tr>
<td>21</td>
<td>PGND</td>
<td>Ground pin for both channels. Power return pin for both channels. Connect returns of both channels' input and output capacitors close to this pin for best noise performance.</td>
</tr>
<tr>
<td>22</td>
<td>IN1</td>
<td>Input supply voltage pin for channel 1 step-down regulator. Connect both IN1 pins together. Connect the input capacitor close to this pin for best noise performance.</td>
</tr>
</tbody>
</table>
Pin Configuration

TQFN45-24
(Top View)

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{IN(HI)}}$</td>
<td>IN1, EN1, LX1 to GND</td>
<td>-0.3 to 30.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{IN(LO)}}$</td>
<td>IN2, VL1 to GND</td>
<td>-0.3 to 6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BST1-LX1}}$</td>
<td>BST1 to LX1</td>
<td>-0.3 to 6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{CONTROL}}$</td>
<td>FB1, COMP1, RS1, OS1, OUT2, DL1 to GND</td>
<td>-0.3 to $V_{\text{IN(LO)}}$ + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{EN2}}$</td>
<td>EN2 to GND</td>
<td>-0.3 to $V_{\text{EN2}}$ + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating Junction Temperature Range</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{\text{LEAD}}$</td>
<td>Maximum Soldering Temperature (at leads, 10 sec)</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>

Thermal Information

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_D$</td>
<td>Maximum Power Dissipation</td>
<td>3.0</td>
<td>W</td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>Thermal Resistance</td>
<td>33</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board with exposed paddle connected to ground plane.
3. Derate 30mW/°C above 25°C ambient temperature.
### Electrical Characteristics

V_{IN1} = 12.0V, V_{IN2} = 3.3V; T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Channel 1: 4.5A Step-Down (Buck) Converter</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IN1}</td>
<td>Input Voltage</td>
<td></td>
<td>6.0</td>
<td>24.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{UVLO1}</td>
<td>UVLO Threshold</td>
<td>V_{IN1} Rising</td>
<td>5.0</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{UVLO1}</td>
<td>V_{IN1} Hysteresis</td>
<td></td>
<td>300</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OUT1}</td>
<td>Output Voltage Range</td>
<td></td>
<td>0.8</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{FB1}</td>
<td>Feedback Pin Voltage</td>
<td></td>
<td>0.576</td>
<td>0.585</td>
<td>0.594</td>
<td>V</td>
</tr>
<tr>
<td>V_{OUT}</td>
<td>Output Voltage Accuracy</td>
<td>I_{OUT} = 0 to 4.5A</td>
<td>-3.0</td>
<td>+3.0</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>(ΔV_{OUT}/ΔV_{IN})</td>
<td>Line Regulation</td>
<td>V_{IN1} = 6V to 24V, V_{OUT1} = 3.3V, I_{OUT1} = 4.5A</td>
<td>0.05</td>
<td>%/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(ΔV_{OUT}/ΔI_{OUT})</td>
<td>Load Regulation</td>
<td>V_{IN1} = 12V, V_{OUT1} = 3.3V, I_{OUT1} = 0A to 4.5A</td>
<td>0.2</td>
<td>%/A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{Q1}</td>
<td>Quiescent Current</td>
<td>V_{EN1} = Low, No load, V_{FB1} = 1.2V</td>
<td>600</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{SHDN1}</td>
<td>Shutdown Current</td>
<td>V_{EN1} = High, V_L = 0V</td>
<td>35</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OCP1}</td>
<td>Over-Current Offset Voltage</td>
<td>V_{EN1} = Low, V_{IN1} = 6.0V to 24.0V, T_A = 25°C</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>mV</td>
</tr>
<tr>
<td>I_{LX1}</td>
<td>LX1 Pin Leakage Current</td>
<td>V_{IN1} = 24.0V, V_{EN1} = 5.0V</td>
<td>-1.0</td>
<td>1.0</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>D_{MAX}</td>
<td>Maximum Duty Cycle</td>
<td></td>
<td>85</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{L1}</td>
<td>Low Side Drive Source Resistance</td>
<td>Pull-Up, V_L = 4.5V</td>
<td>5.0</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{ON1}</td>
<td>Hi Side On-Resistance</td>
<td>Pull-Down, V_L = 4.5V</td>
<td>1.7</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F_{OSC1}</td>
<td>Oscillator Frequency</td>
<td></td>
<td>350</td>
<td>490</td>
<td>650</td>
<td>kHz</td>
</tr>
<tr>
<td>F_{FOLDBACK1}</td>
<td>Short Circuit Foldback Frequency</td>
<td>Current Limit Triggered</td>
<td>100</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{S1}</td>
<td>Start-Up Time</td>
<td>From Enable Channel 1 to Output Regulation</td>
<td>2.5</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel 2: 600mA Low Dropout (LDO) Regulator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IN2}</td>
<td>Input Voltage</td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{DO2}</td>
<td>Dropout Voltage</td>
<td>98% · V_{OUT2(NOM)}, I_{OUT2} = 600mA</td>
<td>1000</td>
<td>1300</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>I_{Q2}</td>
<td>Quiescent (Ground) Current</td>
<td>No load</td>
<td>70</td>
<td>125</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I_{SHDN2}</td>
<td>Shutdown Current</td>
<td>V_{EN2} = GND</td>
<td>1.0</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OUT2(TOL)}</td>
<td>Output Voltage Tolerance</td>
<td>I_{OUT2} = 1mA to 600mA, V_{IN2} = 2.7 to 5.5V, T_A = 25°C</td>
<td>-2.0</td>
<td>+2.0</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I_{OUT2} = 1mA to 600mA, V_{IN2} = 2.7 to 5.5V, T_A = -40°C to 85°C</td>
<td>-3.5</td>
<td>+3.5</td>
<td>%</td>
</tr>
<tr>
<td>e_{N}</td>
<td>Output Noise</td>
<td>BW = 300Hz to 50kHz</td>
<td>250</td>
<td>μVRMS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>I_{OUT2} = 10mA</td>
<td>1kHz</td>
<td>67</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10kHz</td>
<td>47</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1MHz</td>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{LIMIT2}</td>
<td>Current Limit</td>
<td></td>
<td>700</td>
<td>800</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>t_{E2}</td>
<td>Enable Start-Up Delay</td>
<td>From Enable Channel 2 to Output Regulation</td>
<td>15</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Over-Temperature, EN Logic</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_{SD1,2}</td>
<td>Over-Temperature Shutdown Threshold</td>
<td></td>
<td>135</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{ENL1,2}</td>
<td>Enable Threshold Low</td>
<td></td>
<td>0.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{ENH1}</td>
<td>Enable Threshold High</td>
<td></td>
<td>2.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{ENH2}</td>
<td>Input Low Current</td>
<td></td>
<td>1.4</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. The AAT2688 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range and is assured by design, characterization and correlation with statistical process controls.
Typical Characteristics—Channel 1

**Step-Down Converter Efficiency vs. Output Current**
(V\text{OUT1} = 3.3V; \text{L} = 4.7\mu\text{H})

![Efficiency vs. Output Current Graph](chart1)

**Step-Down Converter DC Regulation**
(V\text{OUT1} = 3.3V; \text{L} = 4.7\mu\text{H})

![DC Regulation Graph](chart2)

**Step-Down Converter Output Voltage Error vs. Input Voltage**
(V\text{OUT1} = 3.3V; \text{L} = 4.7\mu\text{H})

![Output Voltage Error Graph](chart3)

**Step-Down Converter Switching Frequency vs. Temperature**
(V\text{IN1} = 12V; \text{VOUT1} = 3.3V; \text{IOUT1} = 4.5A)

![Switching Frequency vs. Temperature Graph](chart4)

**Step-Down Converter Switching Frequency vs. Input Voltage**
(V\text{OUT1} = 3.3V; \text{IOUT1} = 4.5A)

![Switching Frequency vs. Input Voltage Graph](chart5)

**No Load Step-Down Converter Input Current vs. Input Voltage**
(\text{VEN1} = \text{VIN1})

![No Load Input Current Graph](chart6)

DISCONTINUED
Typical Characteristics—Channel 1

Step-Down Converter Output Voltage Error

\[ (V_{IN1} = 12V; V_{OUT1} = 3.3V) \]

\[ \begin{array}{c|cccccc}
\text{Temperature (°C)} & -40 & -15 & 10 & 35 & 60 & 85 \\
\hline
\text{Output Voltage Error (\%)} & -0.6 & -0.4 & -0.2 & 0.0 & 0.2 & 0.4 \\
\end{array} \]

Step-Down Converter Output Ripple

\[ (V_{IN1} = 12V; V_{OUT1} = 3.3V; I_{OUT1} = 4.5A) \]

Step-Down Converter Load Transient Response

\[ (I_{OUT1} = 2.25 \text{ to } 4.5A; V_{IN1} = 12V; C_{OUT1} = 3x22\mu F) \]

Step-Down Converter Load Transient Response

\[ (I_{OUT1} = 0.45 \text{ to } 4.5A; V_{IN1} = 12V; C_{OUT1} = 3x22\mu F) \]

DISCONTINUED
4.5A PMIC Solution for 12V Adapter Systems with 2-Output High Performance Step-Down Converters

Typical Characteristics–Channel 1

**Step-Down Converter Line Transient Response**
(V\textsubscript{IN1} = 6V to 10V; V\textsubscript{OUT1} = 3.3V; I\textsubscript{OUT1} = 4.5A)

**Step-Down Converter Soft Start**
(V\textsubscript{IN1} = 12V; V\textsubscript{OUT1} = 3.3V; I\textsubscript{OUT1} = 4.5A)

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DISCONTINUED
Typical Characteristics—Channel 2

**LDO Input Current vs. Input Voltage**

![Graph showing LDO Input Current vs. Input Voltage](image)

**LDO Dropout Voltage vs. Temperature**

![Graph showing LDO Dropout Voltage vs. Temperature](image)

**LDO Dropout Voltage vs. Output Current**

![Graph showing LDO Dropout Voltage vs. Output Current](image)

**LDO Output Voltage Error vs. Temperature**

![Graph showing LDO Output Voltage Error vs. Temperature](image)

**LDO Dropout Characteristics**

![Graph showing LDO Dropout Characteristics](image)
4.5A PMIC Solution for 12V Adapter Systems
with 2-Output High Performance Step-Down Converters

Typical Characteristics—Channel 2

LDO Turn-Off Response Time
(VIN2 = 3.3V; VEN2 = 3.3V; VOUT2 = 1.8V; IOUT2 = 600mA)

LDO Turn-On Time from Enable
(VIN2 = 3.3V; VEN2 = 3.3V; VOUT2 = 1.8V; IOUT2 = 600mA)

LDO Line Transient Response
(VIN2 = 3V to 4V; VOUT2 = 1.8V; IOUT2 = 600mA; COUT2 = 2.2µF)

LDO Load Transient Response
(IOUT2 = 0.3 to 0.6A; VIN2 = 3.3V; VOUT2 = 1.8V; COUT2 = 2.2µF)

LDO Output Voltage Noise
(IOUT2 = 10mA; Power BW: 300~50KHz)

LDO Power Supply Rejection Ratio, PSRR
(IOUT2 = 10mA; BW: 100KHz to 300KHz)

DISCONTINUED
AAT2688

4.5A PMIC Solution for 12V Adapter Systems with 2-Output High Performance Step-Down Converters

Functional Description

The AAT2688 provides two independently regulated DC outputs; consisting of a high voltage synchronous step-down (Buck) regulator and a low input voltage linear low dropout (LDO) regulator. The PMIC is optimized for low cost 12V adapter inputs, making the device the ideal system-on-a-chip power solution for consumer communications equipment.

Channel 1 is a step-down (Buck) regulator with an input voltage range 6.0 to 24V; providing up to 4.5A output current. 490kHz fixed switching frequency allows small L/C filtering components.

Channel 1 utilizes voltage mode control configured for optimum performance across the entire output voltage and load range. The regulator includes integrated over-current, soft-start and over-temperature protection. Over-current is sensed through the output inductor DC winding resistance. An external resistor network adjusts the current limit according to the DC winding resistance of the desired inductor and the desired output current limit. Frequency reduction limits over-current stresses during short-circuit events. The operating frequency returns to the nominal setting when over-current conditions are removed.

Channel 2 is a low-dropout (LDO) regulator providing up to 600mA output current at a factory set output voltage. The device provides low output noise, low quiescent current, and excellent transient response.

The regulators include integrated over-current, soft-start and over-temperature protection. Independent input and enable pins provide maximum design flexibility.

The AAT2688 is available in the Pb-free 4x5 mm 24-pin TQFN package. The rated operating temperature range is -40°C to 85°C.
Applications Information

Output 1 is a high voltage DC/DC step-down converter providing an output voltage from 0.8V to 5.5V. The integrated high-side N-channel MOSFET device provides up to 4.5A output current. Input voltage range is 6.0V to 24.0V. The step-down converter utilizes constant frequency (PWM-mode) voltage mode control to achieve high operating efficiency while maintaining extremely low output noise across the operating range. High 490kHz (nominal) switching frequency allows small external filtering components, achieving minimum cost and solution size. External compensation and an optional feed forward capacitor allows the designer to optimize the transient response while achieving stability across the operating range.

Output 2 is a low voltage low dropout (LDO) linear regulator providing 1.8V with up to 600mA output current. The input voltage range is 2.7V to 5.5V. The LDO provides very low noise output which can be derived directly from Output 1.

Output Voltage—Channel 1

The output voltage is set using an external resistor divider as shown in Table 1. Minimum output voltage is 0.8V and maximum output voltage is 5.5V. Typical maximum duty cycle is 85%. Example: with R4 = 1.96KΩ,

\[ R3 = \frac{V_{OUT} - 0.585}{0.585} \cdot R4 \]

<table>
<thead>
<tr>
<th>V\text{OUT} (V)</th>
<th>R3 (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>0.715</td>
</tr>
<tr>
<td>1.0</td>
<td>1.37</td>
</tr>
<tr>
<td>1.2</td>
<td>2.05</td>
</tr>
<tr>
<td>1.5</td>
<td>3.09</td>
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<tr>
<td>1.8</td>
<td>4.02</td>
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<td>4.75</td>
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<td>2.5</td>
<td>6.49</td>
</tr>
<tr>
<td>3.0</td>
<td>8.06</td>
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<tr>
<td>3.3</td>
<td>9.09</td>
</tr>
<tr>
<td>5.0</td>
<td>14.7</td>
</tr>
</tbody>
</table>

Table 1: External Resistor Values (Standard 1% Resistors are Substituted for Calculated Values).

1. The R3 and R4 feedback resistors are separate from the compensation network. When changing either R3 and/or R4, the compensation network will have to be altered. Contact the Applications Engineering department for compensation network recommendations for specific output voltages.

Analysis

Channel 1 Regulator Output Capacitor Selection

Three 22μF ceramic output capacitors are required to filter the inductor current ripple and supply the load transient current for \( I_{OUT} = 4.5A \). The 1206 package with 10V minimum voltage rating is recommended for the output capacitors to maintain a minimum capacitance drop with DC bias.

Channel 1 Output Inductor Selection

The step-down converter utilizes constant frequency (PWM-mode) voltage mode control. A 4.7μH inductor value is selected to maintain the desired output current ripple and minimize the converter’s response time to load transients. The peak switch current should not exceed the inductor saturation current or the MOSFETs.

Channel 1 MOSFET Selection

The step-down (buck) converter utilizes synchronous rectification (Q1) for constant frequency (PWM mode) voltage mode control. The synchronous rectifier is selected based on the desired \( R_{DS(on)} \) value and \( Q_s \) (total gate charge), these two critical parameters are weighed against each other. To get a low \( R_{DS(on)} \) value, the MOSFET must be of a very large size and a larger MOSFET will have a large \( Q_s \). Conversely to get a low \( Q_s \), the MOSFET must be small and thus have a large \( R_{DS(on)} \) value. In addition to the trade off between \( R_{DS(on)} \) and \( Q_s \), the maximum voltage rating for the external synchronous MOSFET must exceed the maximum application input voltage value (\( V_{DS(max)} > V_{IN(max)} \)).

The \( Q_s \) affects the turn-on/turn-off time of the synchronous MOSFET, the longer the turn-on/turn-off time the more likely the step-down converter will have “shoot through” current issues. “Shoot through” current occurs when the AAT2688 internal top-side MOSFET and the external synchronous MOSFET are conducting current at the same time. This will result in a low impedance path to ground from the input voltage through the two MOSFETs, and the current may exceed the maximum current rating of the AAT2688 and external synchronous MOSFET. Exceeding the maximum current ratings will lead to the destructive derating of the AAT2688 and external synchronous MOSFET.

DISCONTINUED
The critical parameter recommendations for the external synchronous minimum 25V MOSFET are as follows:

- \( Q_G \) (Total Gate Charge) = 5nC to 15nC (max) (V\text{GS}: 4.5V to 5V)
- \( R_{\text{DS(on)}} \) = 10\,\Omega to 30\,\Omega (max) (V\text{GS}: 4.5V to 5V)

### Channel 1 Input Capacitor Selection

For low cost applications, a 220\,\mu\text{F}/25V electrolytic capacitor is selected to control the voltage overshoot across the high side MOSFET. A small ceramic capacitor with voltage rating at least 1.05 times greater than the maximum input voltage is connected as close as possible to the input pin (Pin 14) for high frequency decoupling.

### Channel 1 Feedback and Compensation Networks

![Figure 1: AAT2688 Feedback and Compensation Networks for Type III Voltage-Mode Control Loop.](image)

The transfer function of the Error Amplifier is dominated by the DC Gain and the \( L \, C_{\text{OUT}} \) output filter of the regulator. This output filter and its equivalent series resistor (ESR) create a double pole at \( F_{\text{PC}} \) and a zero at \( F_{\text{ESR}} \) in the following equations:

\[
\text{Eq. 1: } F_{\text{PC}} = \frac{1}{2 \cdot \pi \cdot R \cdot C_{\text{OUT}}}
\]

\[
\text{Eq. 2: } F_{\text{ESR}} = \frac{1}{2 \cdot \pi \cdot \text{ESR} \cdot C_{\text{OUT}}}
\]

The feedback and compensation networks provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin for system stability. Equation 3, 4, 5 and 6 relate the compensation network’s poles and zeros to the components R1, R3, R5, C5, C6, and C10:

\[
\text{Eq. 3: } F_{P1} = \frac{1}{2 \cdot \pi \cdot R \cdot C_{5} \cdot C_{6}}
\]

\[
\text{Eq. 4: } F_{P2} = \frac{1}{2 \cdot \pi \cdot \text{ESR} \cdot C_{10}}
\]

Components of the feedback, feed forward, compensation, and current limit networks need to be adjusted to maintain the system's stability for different input and output voltage applications as shown in Table 2.

<table>
<thead>
<tr>
<th>Network</th>
<th>Components</th>
<th>( V_{\text{OUT}} = 3.3 , \text{V} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback</td>
<td>R4 1.96kΩ</td>
<td>R3 9.09kΩ</td>
</tr>
<tr>
<td>Feed Forward</td>
<td>R5 150Ω</td>
<td>C10 2.2nF</td>
</tr>
<tr>
<td>Compensation</td>
<td>R1 3.92kΩ</td>
<td>C5 2.2nF</td>
</tr>
<tr>
<td>Current Limit</td>
<td>R6 220nF</td>
<td>R2 2kΩ</td>
</tr>
</tbody>
</table>

Table 2: AAT2688 Feedback, Compensation, and Current Limit Components for \( V_{\text{OUT}} = 3.3 \, \text{V} \).

### Channel 1 Thermal Protection

The AAT2688 has an internal thermal protection circuit which will turn off when the device die temperature exceeds 135°C. The internal thermal protection circuit will actively turn off the high side regulator output device to prevent the possibility of over temperature damage. The Buck regulator output will remain in a shutdown state until the internal die temperature falls back below the 135°C trip point. The combination and interaction between the short circuit and thermal protection systems allows the Buck regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.
**Over-Current Protection**

The regulator provides true-load DC output current sensing which protects the load and limits component stresses. The output current is sensed through the DC resistance in the output inductor. The regulator reduces the operating frequency when an over-current condition is detected; limiting stresses and preventing inductor saturation. This allows the smallest possible inductor for the given application. A small resistor divider may be necessary to adjust the over-current threshold and compensate for variation in inductor DC resistance.

![Resistor Network to Adjust the Current Limit Less than the Pre-Set Over-Current Threshold (Add R7, R8).](image1)

![Resistor Network to Adjust the Current Limit Greater than the Pre-Set Over-Current Level (Add R6, R7).](image2)

**Channel 2 Input Capacitor**

Typically, a 1μF or larger capacitor is recommended for C\textsubscript{IN} in most applications. A C\textsubscript{IN} capacitor is not required for basic LDO regulator operation. However, if the AAT2688 is physically located more than three centimeters from an input power source, a C\textsubscript{IN} capacitor will be needed for stable operation.

C\textsubscript{IN} should be located as close to the device V\textsubscript{IN} pin as possible. C\textsubscript{IN} values greater than 1μF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C\textsubscript{IN}. There is no specific capacitor ESR requirement for C\textsubscript{IN}. However, for 150mA LDO regulator output operation, ceramic capacitors are recommended for C\textsubscript{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources, such as batteries in portable devices.

**Channel 2 Output Capacitor**

For proper load voltage regulation and operational stability, a capacitor is required between pins V\textsubscript{OUT} and GND. The C\textsubscript{OUT} capacitor connection to the LDO regulator ground pin should be connected as close as possible for maximum device performance. The AAT2688 LDO has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1μF to 10μF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the channel 2 should use 2.2μF or greater for C\textsubscript{OUT}. If desired, C\textsubscript{OUT} may be increased without limit. In low output current applications where output load is less than 10mA, the minimum value for C\textsubscript{OUT} can be as low as 0.47μF.

**Channel 2 Enable Function**

The AAT2688 features an LDO regulator enable/disable function. This pin (EN) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V\textsubscript{IN} to keep the LDO regulator in a continuously on state. When the LDO regulator is in shut-
down mode, an internal 1.5kΩ resistor is connected between V\text{OUT} and GND. This is intended to discharge C\text{OUT} when the LDO regulator is disabled. The internal 1.5kΩ has no adverse effect on device turn-on time.

**Channel 2 Short-Circuit Protection**

The AAT2688 LDO contains an internal short-circuit protection circuit that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or LDO regulator package power dissipation exceeds the device thermal limit.

**Channel 2 Thermal Protection**

The AAT2688 LDO has an internal thermal protection circuit which will turn on when the device die temperature exceeds 135°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of over temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 135°C trip point. The combination and interaction between the short circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

**Channel 2 No-Load Stability**

The AAT2688 is designed to maintain output voltage regulation and stability under operational no load conditions. This is an important characteristic for applications where the output current may drop to zero.

**Channel 2 Reverse Output-to-Input Voltage Conditions and Protection**

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage, maintaining a reverse bias on the internal parasitic diode. Conditions where V\text{OUT} might exceed V\text{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V\text{OUT} pin, possibly damaging the LDO regulator. In applications where there is a possibility of V\text{OUT} exceeding V\text{IN} for brief amounts of time during normal operation, the use of a larger value C\text{IN} capacitor is highly recommended. A larger value of C\text{IN} with respect to C\text{OUT} will affect a slower C\text{IN} decay rate during shutdown, thus preventing V\text{OUT} from exceeding V\text{IN}. In applications where there is a greater danger of V\text{OUT} exceeding V\text{IN} for extended periods of time, it is recommended to place a Schottky diode across V\text{IN} to V\text{OUT} (connecting the cathode to V\text{IN} and anode to V\text{OUT}). The Schottky diode forward voltage should be less than 0.45V.

**Thermal Calculations**

There are three types of losses associated with the AAT2688 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the R\text{DS(ON)} characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the synchronous step-down converter and LDO losses is given by:

\[
P_{\text{total}} = \frac{I_{\text{OUT1}}^2 \cdot (R_{\text{DS(ON)H}} \cdot V_{\text{OUT1}} + R_{\text{DS(ON)L}} \cdot (V_{\text{IN1}} - V_{\text{OUT1}}))}{V_{\text{IN1}}} + (t_{\text{SW}} \cdot F_S \cdot I_{\text{OUT1}} + I_{Q1} \cdot V_{\text{IN1}} + (V_{\text{IN2}} - V_{\text{OUT2}}) \cdot I_{\text{OUT2}})
\]

I_{Q1} and I_{Q2} are the step-down converter and LDO quiescent currents respectively. The term t_{SW} is used to estimate the full load step-down converter switching losses.

For a synchronous Step-Down converter, the power dissipation occurs in the internal high side MOSFET during the on time and the external low side MOSFET during the off time. When the internal high side switch is on, the power dissipates on the external low side switch. The total package losses for AAT2688 reduce to the following equation:

\[
P_{\text{total}} = \frac{I_{\text{OUT1}}^2 \cdot R_{\text{DS(ON)H}} \cdot D + (t_{\text{SW}} \cdot F_S \cdot I_{\text{OUT1}} + I_{Q1}) \cdot V_{\text{IN}} + (V_{\text{IN2}} - V_{\text{OUT2}}) \cdot I_{\text{OUT2}}}{V_{\text{IN}}}
\]

Where: D = \frac{V_{\text{OUT}}}{V_{\text{IN}}}

Since R\text{DS(ON)} quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the \theta_{JA} for the TQFN45-24 package, which is 33°C/W.

\[
T_{J(\text{MAX})} = P_{\text{TOTAL}} \cdot \theta_{JA} + T_{\text{AMB}}
\]
**Layout Considerations**

The suggested PCB layout for the AAT2688 is shown in Figures 5 through 8. The following guidelines should be used to help ensure a proper layout.

1. The power input capacitors (C1 and C15) should be connected as close as possible to high voltage input pin (IN1) and power ground.
2. C1, L1, Q1, C7, C8, and C9 should be placed as close as possible to minimize any parasitic inductance in the switched current path which generates a large voltage spike during the switching interval. The connection of inductor to switching node should be as short as possible.
3. The feedback trace or FB1 pin should be separated from any power trace and connected as close as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load returns to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect unused signal pins to ground or input to avoid unwanted noise coupling.
6. The critical small signal components include feedback components, and compensation components should be placed close to the FB1 and COMP1 pins. The feedback resistors should be located as close as possible to the FB1 pin with its ground tied straight to the signal ground plane which is separated from power ground plane.
7. C4 should be connected close to the RS1 and OS1 pins, while R2 should be connected close to the inductor.
8. R7 should be connected directly to the output pin of inductor L1 to sense precisely its DCR.
9. For good thermal coupling, a 4-layer PCB layout is recommended and PCB vias are required from the exposed pad (EP) for the TQFN45-24 paddle to the middle plane and bottom plane. The EP is internally connected to IN.

![Figure 4: AAT2688 Evaluation Board Schematic for VIN = 6V-24V and VOUT = 3.3V.](image-url)
AAT2688

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Figure 5: AAT2688IFK Evaluation Board Top Layer.

Figure 6: AAT2688IFK Evaluation Board Mid1 Layer.

Figure 7: AAT2688IFK Evaluation Board Mid2 Layer.

Figure 8: AAT2688IFK Evaluation Board Bottom Layer.
AAT2688 Design Example

Specifications

- $V_{O1} = 3.3V \, @ \, 4.5A$, Pulsed Load $\Delta I_{LOAD} = 4.5A$
- $V_{O2} = 1.8V \, @ \, 600mA$
- $V_{IN1} = 12V$
- $F_s = 490kHz$
- $T_{AMB} = 85^\circ C$ in TQFN45-24 package

Channel 1 Output Inductor

For Sumida inductor RCH108NP-4R7M, $4.7 \mu H$, $DCR = 11.7m\Omega$ max.

\[
\Delta I = \frac{V_{OUT1}}{L_1 \cdot F_s} \left(1 - \frac{V_{OUT1}}{V_{IN1}}\right) = \frac{3.3V}{4.7\mu H \cdot 490kHz} \cdot \left(1 - \frac{3.3V}{12V}\right) = 1A
\]

\[I_{PK1} = I_{OUT1} + \frac{\Delta I}{2} = 4.5A + 1A = 5.5A\]

\[P_{L1} = I_{OUT1}^2 \cdot DCR = 5.5A^2 \cdot 11.7m\Omega = 354mW\]

Channel 1 Output Capacitor

$V_{DROOP} = 0.4V$

\[C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_s} = \frac{3 \cdot 4.5A}{0.4V \cdot 490kHz} = 69\mu F; \, use \, 3x22\mu F\]

\[I_{RMS(MAX)} = \frac{1}{2 \sqrt{3}} \cdot \frac{V_{OUT1} \cdot (V_{IN(MAX)} - V_{OUT1})}{L \cdot F_s \cdot V_{IN(MAX)}} = \frac{1}{2 \sqrt{3}} \cdot \frac{3.3V \cdot (24V - 3.3V)}{4.7\mu H \cdot 490kHz \cdot 24V} = 357mA_{RMS}\]

\[P_{RMS} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot (357mA)^2 = 0.6W\]

Channel 1 Input Capacitor

Input Ripple $V_{PP} = 33mV$

\[C_{IN1} = \frac{1}{\left(\frac{V_{PP}}{I_{OUT1} \cdot ESR}\right) \cdot 4 \cdot F_s} = \frac{1}{\left(\frac{33mV}{4.5A} - 5m\Omega\right) \cdot 4 \cdot 490kHz} = 219\mu F\]

For low cost applications, a $220\mu F/25V$ electrolytic capacitor in parallel with a $1\mu F/25V$ ceramic capacitor is used to reduce the ESR.

\[I_{RMS} = \frac{I_{OUT1}}{2} = 2.25A\]

\[P = ESR \cdot (I_{RMS})^2 = 5m\Omega \cdot (2.25A)^2 = 25.3mW\]
**AAT2688**

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### Channel 1 Current Limit

Voltage sense $V_s = 100$mV  
Total trace parasitic resistor and inductor DCR $= 10$mΩ

\[
I_{\text{PRESET}} = \frac{V_s}{\text{DCR}} = \frac{100\text{mV}}{10\text{mΩ}} = 10\text{A} \geq I_{\text{LIMIT}}
\]

\[
R_8 = \frac{V_{\text{OUT}} \cdot R_2}{V_s - I_{\text{LIMIT}} \cdot \text{DCR}} = \frac{3.3\text{V} \cdot 2\text{kΩ}}{0.1\text{V} - 6\text{A} \cdot 10\text{mΩ}} = 165\text{kΩ}
\]

\[
R_7 = \frac{R_2 \cdot R_8}{R_8 - R_2} = \frac{2\text{kΩ} \cdot 165\text{kΩ}}{165\text{kΩ} - 2\text{kΩ}} = 2\text{kΩ}
\]

### AAT2688 Losses

All values assume 25°C ambient temperature and thermal resistor of 50°C/W in the TQFN45-24 package.

\[
P_{\text{TOTAL}} = I_{\text{OUT1}}^2 \cdot R_{\text{DS(OFF)}} \cdot D + (t_{\text{SW}} \cdot F_s \cdot I_{\text{OUT1}} + I_0) \cdot V_{\text{IN}} + (V_{\text{IN2}} - V_{\text{OUT2}}) \cdot I_{\text{OUT2}}
\]

\[
P_{\text{TOTAL}} = \frac{4.5\text{A}^2 \cdot 70\text{mΩ} \cdot 3.3\text{V}}{12\text{V}} + (5\text{ns} \cdot 490kHz \cdot 4.5\text{A} + 70\mu\text{A}) \cdot 12\text{V} + (3.3 - 1.8) \cdot 600\text{mA}
\]

\[
P_{\text{TOTAL}} = 1.42\text{W}
\]

\[
T_{\text{J(MAX)}} = T_{\text{AMB}} + \Theta_{\text{JA}} \cdot P_{\text{LOSS}} = 85°C + (33°C/\text{W}) \cdot 1.42\text{W} = 131°C
\]

DISCONTINUED
AAT2688

4.5A PMIC Solution for 12V Adapter Systems with 2-Output High Performance Step-Down Converters

Ordering Information

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<th>Package</th>
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<th>Channel 2</th>
<th>Marking¹</th>
<th>Part Number (Tape and Reel)²</th>
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Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to Skyworks Definition of Green™, document number SQ04-0074.

Legend

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<tr>
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<td>A</td>
</tr>
<tr>
<td>1.8</td>
<td>I</td>
</tr>
</tbody>
</table>

Package Information

1. XYY = Assembly and date code.
2. Sample stock is generally held on part numbers listed in BOLD.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

All dimensions in millimeters.
AAT2688

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